IN THE CLAIMS

Please cancel claims 20-25. The claims are as follows:

1. (ORIGINAL) A method of determining a location of an I_{DDQ} defect within an area of an integrated circuit having a substrate and a plurality of terminals arranged on a surface of said substrate, said area provided with and bounded by corresponding ones of said plurality of terminals, the method comprising the steps of:

activating an I_{DDQ} defect to generate I_{DDQ} defect current within said integrated circuit;

measuring amounts of said I_{DDQ} defect current at said corresponding terminals bounding said area; and

determining the location of the I_{DDQ} defect based on said amounts of said I_{DDQ} defect current measured at said corresponding terminals.

2. (ORIGINAL The method of claim 1, wherein the determining step further comprising the steps of:

dividing said area into a plurality of subsections, each subsection provided with a corresponding one of said terminals bounding said area; and

determining which subsection includes said I_{DDQ} defect based on said amounts of said I_{DDQ} defect current measured at said corresponding terminals.

3. (ORIGINAL) The method of claim 2, further comprising steps of:

selecting one of said subsections determined to include said I_{DDQ} defect;

dividing said selected subsection into a plurality of sub-subsections; and

determining which sub-subsection includes said I_{DDQ} defect based on a ratio between an amount of I_{DDQ} defect current forwarded toward one of said terminals provided for said selected subsection and an amount of a sum of said I_{DDQ} defect current measured at said terminals bounding said area.

4. (ORIGINAL) The method of claim 3, wherein said plurality of subsections are arranged in a matrix of X rows and Y columns within said area, and said plurality of sub-sections are arranged in a matrix of M rows and N columns,
wherein said X, Y, M and N are natural numbers.

5. (ORIGINAL) The method of claim 4, wherein said step of determining which sub-section includes said I_{DDQ} defect comprising the steps of:

determining which row of said selected subsection includes said I_{DDQ} defect based on a ratio between (a) an amount of a sum of said I_{DDQ} defect current measured at said terminal provided for said selected subsection and at a first neighboring terminal provided for one of said subsections arranged on a same row with said selected subsection and (b) said amount of said sum of said I_{DDQ} defect current measured at said terminals bounding said selected area; and

determining which column of said selected subsection includes said I_{DDQ} defect based on a ratio between (a) an amount of a sum of said I_{DDQ} defect current measured at said terminal provided for said selected subsection and at a second neighboring terminal provided for one of said subsections arranged on a same column with said selected subsection and (b) said amount of said sum of said I_{DDQ} defect current measured at said terminals bounding said selected area.

6. (ORIGINAL) A method for testing an integrated circuit substrate having a plurality of terminals on a surface thereof, the method comprising the steps of:

dividing said surface into a plurality of areas;

activating an I_{DDQ} defect to generate I_{DDQ} defect current within said integrated circuit; and

measuring an amount of said I_{DDQ} defect current generated within each area.

7. (ORIGINAL) The method of claim 6, wherein each area has at least one terminal corresponding thereto.

8. (ORIGINAL) The method of claim 6, further comprising the step of determining whether each area includes said I_{DDQ} defect based on said amount of said I_{DDQ} defect current measured at said at least one terminal.

9. (ORIGINAL) The method of claim 8, wherein said determining step includes the step of comparing the I_{DDQ} defect current measured at each area with a preselected value.

10. (ORIGINAL) The method of claim 8, further comprising the step of determining a location of said I_{DDQ} defect within said integrated circuit substrate.

11. (ORIGINAL) The method of claim 10, wherein said step of determining the location of said I_{DDQ} defect comprises the steps of:

selecting one of said areas determined to include said I_{DDQ} defect;

dividing said selected area into a plurality of subsections, each subsection provided with a corresponding one of said terminals bounding said selected area; and

determining which subsection includes said I_{DDQ} defect based on said amount of the I_{DDQ} defect current measured at said terminals bounding said selected area.

12. (ORIGINAL) The method of claim 11, further comprising the steps of:

selecting one of said subsections determined to include said I_{DDQ}defect;

dividing said selected subsection into a plurality of sub-subsections; and

determining which sub-subsection includes said I_{DDQ} defect based on the ratio between (a) an amount of said I_{DDQ} defect current forwarded to said terminal provided for said selected subsection and (b) an amount of a sum of said I_{DDQ} defect current measured at said terminals bounding said selected area.

13. (ORIGINAL) The method of claim 12, wherein said plurality of subsections are arranged in a matrix of X rows and Y columns within said selected area, and said plurality of sub-subsections are arranged in a matrix of M rows and N columns within said selected subsection, wherein X, Y,

M and N are natural numbers.

14. (ORIGINAL) The method of claim 13, wherein said step of determining which sub-subsection includes said I_{DDQ} defect comprises the steps of:

determining which row of said selected subsection includes said I_{DDQ} defect based on a ratio between (a) an amount of a sum of said I_{DDQ} defect current measured at said terminal provided for said selected subsection and at a first neighboring terminal provided for one of said subsections arranged on a same row with said selected subsection and (b) said amount of said sum of said I_{DDQ} defect current measured at said terminals bounding said selected area; and

determining which column of said selected subsection includes said I_{DDQ} defect based on a ratio between (a) an amount of a sum of said I_{DDQ} defect current measured at said terminal provided for said selected subsection and at a second neighboring terminal provided for one of said subsections arranged on a same column with said selected subsection and (b) said amount of said sum of said I_{DDQ} defect current measured at said terminals bounding said selected area.

15. (ORIGINAL) A method for testing an integrated circuit substrate having a plurality of terminals on a surface thereof, the method comprising the steps of:

dividing said surface into a plurality of areas, each area provided with at least one of said plurality of terminals;

activating an I_{DDQ} defect to generate I_{DDQ} defect current within said integrated circuit; and

measuring an amount of said I_{DDQ} defect current generated within each area;

creating an I_{DDQ} current map of said integrated device based on said amounts of said I_{DDQ} defect current measured at said plurality of terminals;

determining whether each area includes said I_{DDQ} defect based on said I_{DDQ} current map; and

determining a location of said I_{DDQ} defect within said integrated circuit substrate based on said I_{DDQ} current map.

16. (ORIGINAL) The method of claim 15, further comprising the step of isolating said I_{DDQ} defect within said integrated circuit substrate.

17. (ORIGINAL) The method of claim 15, wherein said testing method is performed on a plurality of integrated circuit substrates to create a plurality of I_{DDQ} current maps.

18. (ORIGINAL) The method of claim 17, further comprising step of determining an I_{DDQ} defect candidate area among said plurality of areas based on said plurality of I_{DDQ} current maps.

19. (ORIGINAL) A method for diagnosing a location of an I_{DDQ} defect in an integrated circuit

substrate having a plurality of terminals on a surface thereof, the method comprising the steps of:

dividing said surface into a plurality of areas, each area being provided with at least one of said plurality of terminals;

applying a plurality of test patterns to said integrated circuit substrate, each test pattern placing said integrated circuit into a different electrical state;

measuring an amount of current generated in each area of said integrated circuit substrate during each test pattern applied thereto;

determining which of said plurality of test patterns activate the I_{DDQ} defect and which of said plurality do not activate the I_{DDQ} defect based on the measured amount of the current generated in each area; and

using the determination result for said test patterns as data input to a diagnostic tool capable of modeling various I_{DDQ} defects and comparing a predicted activation behavior to said determination results.

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